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Cutting Simulation – one basis for coating-substrate-optimization

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Abstract:
Compared to standard machining procedures, workpieces in high-performance cutting are machined at higher speeds, with larger loads and at a higher feed rate. The aim is to achieve a large chipping rate. Compared to straightforward high-speed cutting (HSC) – that is, machining at a high cutting rate – HPC generally involves lower cutting speeds and significantly larger cut depths. In addition to the machining process itself, HPC generally also integrates all the other factors involved in production. The objective is to ensure maximum productivity and performance reliability
Users do significantly better with robust precision cutting tools that also provide a generous dose of intelligence with their design, statically and dynamically strength and a long life time due to excellent coating-substrate-systems.
The main goal of the paper is to present newest research activities dealing with a closed-loop design of coating-substrate-systems, based on the chip formation simulation around the cutting edge. This can be used for Virtual Coating-Substrate-Systems Design. The investigations are part within the M3-2S Project.
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Keywords: Coating-Substrate-Systems, Cutting Tool, Simulation, Manufacturing

1. Introduction

During the development of a new cutting tool generation usually several design variants are taken into consideration. But, the manufacturing of prototypes is very time and cost expensive. Modeling and simulation can be used to reduce this cost. On the other hand, simulations based on numerical models need geometric and material data given from CAD data files and boundary load conditions given by the process. To get a cost reduction in the design process, numerical calculations as part of the developing process of compli-

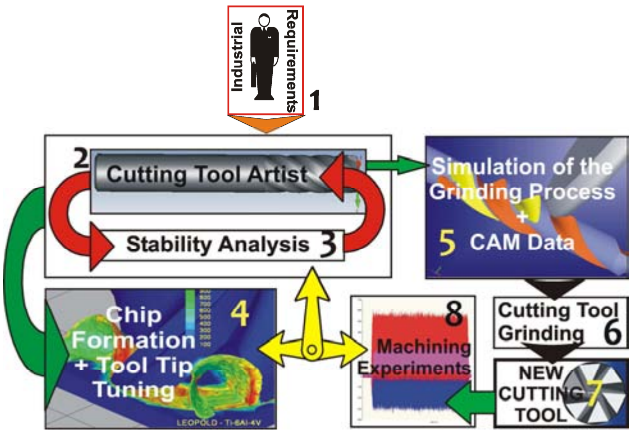


Figure 1: The closed-loop cutting tool design [1]

-cated cutting tools are necessary for a fast cutting tool design and manufacturing process.

In comparison with high-speed cutting (HSC), in high-performance cutting (HPC) the feed will increase in addition to the cutting speed [2]. Under these conditions, the cutting tools are loaded more heavy than in "conventional" high-speed cutting [3].

Later on a lot of papers have been published to improve selected properties of cutting tools [4, 5, 6, 7].

To reduce the time-to-market in case of new cutting tool applications, the insulated consideration is no longer appropriate. So, the main focus of this paper is directed in addition to the industrial realized closed-loop-cutting tool design (Fig. 1) – the next step forward is the **V**irtual **C**oating-**S**ubstrate-**S**ystem **D**esign (**VCSSD**).

2. Cutting Tool Design

Based on the industrial requirements (number 1 in Fig. 1), the Cutting Tool Artist (CAD Designer) will start with a preliminary design of the new tool.

The industrial requirements where focused to:

a. multivalent application in the shop floor
b. high tool life
c. high surface quality, also under unstable machining conditions
d. high chip rate with small chips for a easy evacuation

The Cutting Tool Design Process is based on the VDI guideline 2206. Due to the industrial requirements for a high chip rate, the flute volume should be as high as possible. In contrast to this requirement, the mechanical stability of the cutting tool will be reduced. To avoid forced vibrations and cutting tool breakage, the stress-strain condition of the draft design is usually investigated with a finite-element simulation. At this moment, the multiscale simulation of coating-substrate-systems are not commonly applied in the industry.

3. The industrial demonstrator

The demonstrator by the project partner Fundiciones del Estanda S.A. is an internal turning process for an electromagnetic brake (Fig. 2).

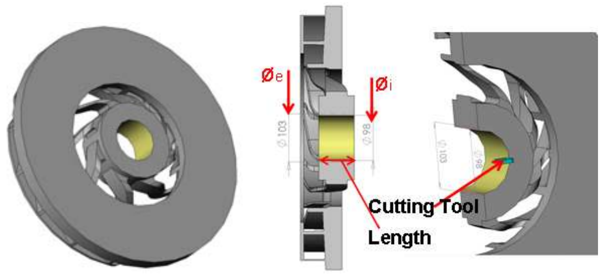


Figure 2: Electromagnetic brake

The cutting conditions are:
Cutting speed : 76 rpm; Feed: 0,4mm/rpm
Φ_i = 98 mm; Φ_e = 103 mm
Workpiece Material : 20NiCrMo2-2
For the Cutting Insert a SPMR 120308 type was used and the following coatings has been selected: TiN; Tin and CrN Monolayer as well as a TiN-CrN Superlattice Coating.

4. FE Simulation of Chip Formation

There are two fundamental approaches to FE cutting process simulation: the displacement or Lagrangian formulation and the flow or Eulerian one.
For the investigations inside in this project the FE-Code “AdvantEdge™” [8] was used. This is an explicit dynamic, thermo-mechanically coupled finite element modeling package specialized for metal cutting. The principle is pointed out in the following equations

The balance of linear momentum is written as[1]:

$$\sigma_{ij,j} + \rho b_i = \rho \ddot{u}_i \tag{1}$$

Thermal Equations
Heat generation and transfer are handled via the second law of thermodynamics. A discretized weak form of the first law is given by

$$C\dot{T}_{n+1} + KT_{n+1} = Q_{n+1} \tag{2}$$

where **T** is the array of nodal temperatures,

$$C_{ab} = \int_{Bt} c\rho N_a N_b dV_o \tag{3}$$

is the heat capacity matrix

$$K_{ab} = \int_{B0} D_{ij} N_{a,i} N_{b,j} dV \tag{4}$$

is the conductivity matrix

$$Q_a = \int_{Bt} sN_a dV + \int_{B\tau q} hN_a dS \tag{5}$$

is the heat source array with h having the appropriate for the chip or tool. In machining applications, the main sources of heat are plastic deformation in the bulk and frictional sliding at the tool-workpiece interface.

Constitutive model and material characterization

In order to model chip formation, constitutive modeling for metal cutting requires determination of material properties at high strain rates, large strains, and short heating times and is quintessential for prediction of segmented chips due to shear- localization. The increase in flow stress is due to strain rate sensitivity is accounted for with the relation

$$\left(1 + \frac{\dot{\varepsilon}^p}{\dot{\varepsilon}_0{}^p}\right) = \left(\frac{\bar{\sigma}}{g(\varepsilon^p)}\right)^{m_1} \tag{7}$$

where $\bar{\sigma}$ is the effective Mises stress, g the flow stress, $\bar{\varepsilon}^p$ the accumulated plastic strain, $\dot{\varepsilon}_0$ a reference plastic strain rate, and m_1 is the strain rate sensitivity exponent. A power hardening law model is adopted with thermal softening. This gives

$$g = \sigma_0 \Theta(T) \left(1 + \frac{\varepsilon^p}{\varepsilon_0^p}\right)^{1/n} \tag{8}$$

where n is the hardening exponent, T the current temperature, and σ_0 is the initial yield stress at the reference temperature T_0 , ε_0^p the reference plastic strain, and Θ (T) is a thermal softening factor ranging from 1 at room temperature to 0 at melt and having the appropriate variation in between.
This FE-Code has been used to calculate the mechanical-thermal loading at the cutting tool.

5. Numerically Investigations

The Chip Formation process is in general a three dimensional process. In a first step, the complete 3D – internal turning process has been investigated. We used a high-resolution FE-net with the lowest element size up to 5µm.
With the following results, the project partner University of Strathclyde calculated the risk for coating damage. A model developed for the analysis of failures of multi layer coated surfaces subjected to the indentation [9] is extended to the surface-damage analysis of a cutting tool. The model is constituted of two parts - a TiN coating (2 µm thick) and a Silicon Nitrided substrate. In order to study the potential damages of the coated tool-surface, a series of cohesive elements were used between continuum elements in the model of the coating layer. The analysis

[1] We are using the same symbols given in the Theoretical Manual from Third Wave *AdvantEdge™*

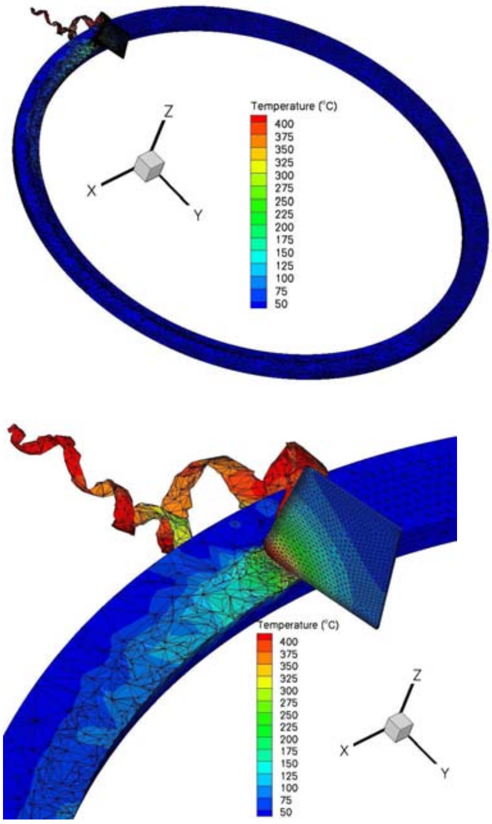
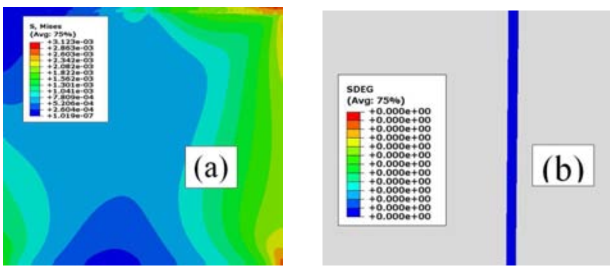


Figure 3: FE Model for the 3D-internal turning process

was conducted in two steps: (i). a coupled temperature-displacement analysis with a global model which examined the temperature distribution and residual stresses in the tool; and (ii). a static analysis with a submodel which included cohesive elements for the damage analysis. The temperature distribution along the depth of the cutting tool, computed based on the surface temperature , the Mises Stress and the pressure obtained in the cutting simulation performed by TBZ based on the model Figure 3. The analysis suggested that although a stress of more than 3000 MPa could occur in the coating (Fig. 4(a)) no damage-initiation was observed for the thermal and mechanical loading applied (the damage coefficient is zero in Fig. 4(b)) - the maximum separation in the coating surface reached up to 0.005 (Fig. 4(c)), which is much less than the critical value of 0.01 on the initiation of damage, prescribed for the TiN coating.



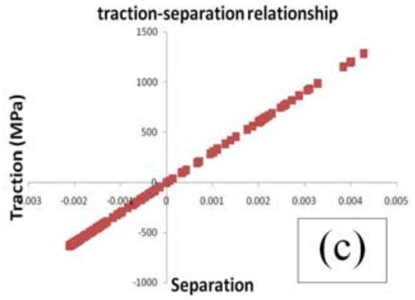


Figure 4: (a) Mises stress; (b) Damage coefficient; (c) Traction-separation relationship for a cohesive element in the coating.

Due to the long calculation time (180° cutting tool rotation takes about 17h), in an second step the more simplified Nose turning process has been investigated.

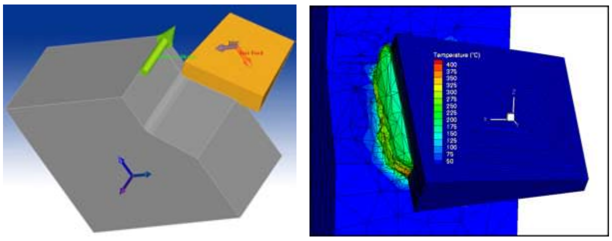


Figure 5: Nose turning

The calculation time can be reduced up to 6h for 3mm turning operation.
Finally, a 2D-Turning Model (Orthogonal Cutting – app. 3h for 3mm) has been used to get faster results for the influence of the different coating-substrate-systems.

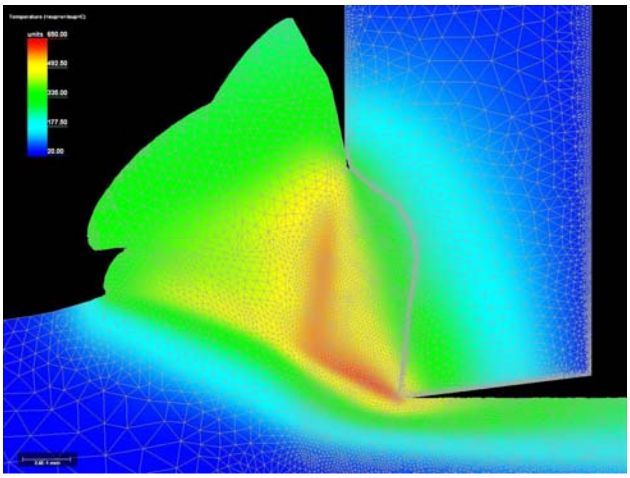


Figure 6: Orthogonal Cutting Model

The numerically investigations has been focused to standard tools (cemented carbide) without coatings, TiN coatings; superlattice TiN-CrN coatings and for comparison a cutting tool with two monolayer coatings : TiN + CrN.
For the cutting forces, the practically well know results has been verified – the superlattice coating tends to reduced cutting forces (Figure 7) and the temperature at in the chip near the cutting tool is higher than other one – so the mechanically and thermal loading of the cutting

tool is less. With other detailed investigations, which will be reported inside in the M3-2S project – superlattice coatings can be used to reduce the tool wear and to increase the lifetime of the cutting tool.

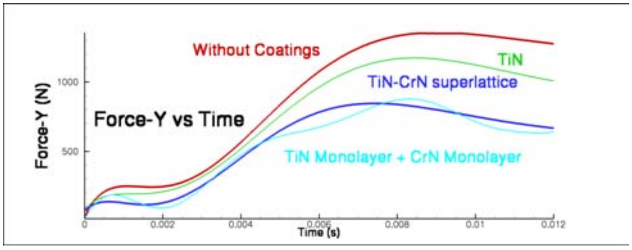


Figure 7: Calculated Cutting Forces for different coatings

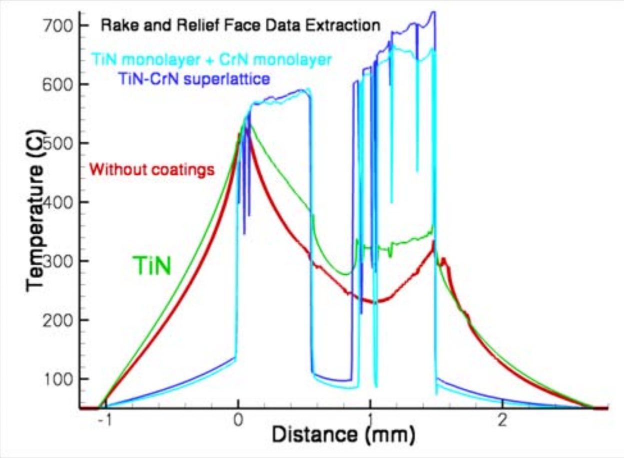


Figure 8: Temperature distribution in the chip near the tool (-1<l<0:relief face; 0<l<3: rake face)

Based on this high precise chip-formation simulation, the mechanical and thermal loading along the rake- and relief face of the cutting tool can bed determined and are the main boundary conditions for the stability analysis and crack prediction within the coatings [11].

6. Conclusion

How are tools engineered right now? It often goes as follows: a model of the tool and the coating is developed and a prototype is ground and analyzed. Results are then evaluated by development engineers together with costumers who make appropriate changes to the tool geometry. A new prototype is developed, and the cycle is repeated. Each single iteration demands high costs in terms of personnel, materials and machine time.

The closed-loop system enables users to relocate the prototyping process from the machine tool onto a personal computer, keeping machine tests to a minimum. The time-to-market can strongly reduced.

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